(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
29 November 2001 (29.11.2001)

PCT

(10) International Publication Number
WO 01/91181 A2

(51) International Patent Classification[7]: H01L 21/768

(21) International Application Number: PCT/US01/15991

(22) International Filing Date: 18 May 2001 (18.05.2001)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
09/577,705 23 May 2000 (23.05.2000) US

(71) Applicant: APPLIED MATERIALS, INC. [US/US]; P.O. Box 450A, Santa Clara, CA 95052 (US).

(72) Inventors: LEE, Wei, Ti; 2841 Rubino Circle, San Jose, CA 95125 (US). GUO, Ted; 3156 Morris Drive, Palo Alto, CA 94303 (US). YAO, Gongda; 44875 Winding Lane, Fremont, CA 94539 (US).

(74) Agents: BERNADICOU, Michael, A. et al.; Blakely, Sokoloff, Taylor & Zafman LLP, 7th floor, 12400 Wilshire Boulevard, Los Angeles, CA 90025 (US).

(81) Designated States *(national)*: JP, KR.

(84) Designated States *(regional)*: European patent (AT, BE, CH, CY, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE, TR).

Published:
— *without international search report and to be republished upon receipt of that report*

For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.

WO 01/91181 A2

(54) Title: LINER MATERIALS

(57) Abstract: A method for metallizing integrated circuits is disclosed. In one aspect, an integrated circuit is metallized by depositing liner material on a substrate followed by one or more metal layers. The liner material is selected from the group of tantalum (Ta), tantalum nitride (TaN), niobium (Nb), niobium nitride (NbN), vanadium (V), vanadium nitride (VN), and combinations thereof. The liner material is preferably conformably deposited on the substrate using physical vapor deposition (PVD). The one or more metal layers are deposited on the barrier layer using chemical vapor deposition (CVD), physical vapor deposition (PVD), or a combination of both CVD and PVD.

LINER MATERIALS

BACKGROUND OF THE DISCLOSURE

1. Field of the Invention

The present invention relates to liner materials and, more particularly the use of liner materials in integrated circuit fabrication.

2. Description of the Background Art

Integrated circuits have evolved into complex devices that can include millions of components (e. g., transistors, capacitors and resistors) on a single chip. The evolution of chip designs continually requires faster circuitry and greater circuit density. The demands for greater circuit density necessitate a reduction in the dimensions of the integrated circuit components.

As the dimensions of the integrated circuit components are reduced (e. g., sub-micron dimensions), the materials used to fabricate such components contribute to the electrical performance of such components. For example, low resistivity metal interconnects (e. g., aluminum and copper) provide conductive paths between the components on integrated circuits. Typically, the metal interconnects are electrically isolated from each other by an insulating material.

Additionally, a liner material often separates the metal interconnects from the insulating material. The liner material can be a barrier layer to inhibit the diffusion of the metal into the insulating material. Diffusion of the metal into the insulating material is undesirable because such diffusion can affect the electrical performance of the integrated circuit, or render it inoperative. Alternatively, the liner material can be a nucleation layer (e. g., wetting layer) to which the interconnect metallization is adherent.

A combination of titanium (Ti) and/or titanium nitride (TiN), for example, is often used for the liner material. However, at high temperatures (e. g., temperatures greater than about 400 °C) Ti and/or TiN may react with Al to form titanium tri-aluminide ($TiAl_3$). The formation of the $TiAl_3$ reduces the effective linewidth of the aluminum interconnects which undesirably increases the resistance of such interconnects and degrades the overall performance of the integrated circuit.

Therefore, a need exists in the art for integrated circuit metallization schemes including liner materials that are non-reactive with the metals used to form interconnects.

SUMMARY OF THE INVENTION

The present invention provides a method for metallizing integrated circuits. In one aspect, an integrated circuit is metallized by depositing liner material on a substrate followed by one or more metal layers. The liner material is selected from tantalum (Ta), tantalum nitride (TaN), niobium (Nb), niobium nitride (NbN), vanadium (V), vanadium nitride (VN), and combinations thereof. The liner material is preferably conformably deposited on the substrate using physical vapor deposition (PVD). The one or more metal layers are conformably deposited on the liner material using chemical vapor deposition (CVD), physical vapor deposition (PVD), or a combination of both CVD and PVD.

In another aspect, a damascene interconnect is fabricated. In one embodiment, a process sequence includes providing a substrate with one or more dielectric layers thereon. The one or more dielectric layers on the substrate, have apertures defined therein. Liner material selected from tantalum (Ta), tantalum nitride (TaN), niobium (Nb), niobium nitride (NbN), vanadium (V), vanadium nitride (VN), and combinations thereof is conformably deposited on the one or more dielectric layers. Thereafter, the damascene interconnect is formed when one or more metal layers are conformably deposited on the liner material. The liner material is preferably conformably deposited on the substrate using physical vapor deposition (PVD). The one or more metal layers are conformably deposited on the barrier layer using chemical vapor deposition (CVD), physical vapor deposition (PVD), or a combination of both CVD and PVD.

BRIEF DESCRIPTION OF THE DRAWINGS

The teachings of the present invention can be readily understood by considering the following detailed description in conjunction with the accompanying drawings, in which:

FIG. 1 depicts a schematic illustration of an apparatus that can be used for the practice of this invention;

FIG. 2 depicts a schematic cross-sectional view of a sputtering type physical vapor deposition (PVD) chamber;

FIG. 3 depicts a schematic cross-sectional view of a plasma enhanced chemical vapor deposition (CVD) chamber; and

FIGS. 4a-4d illustrate schematic cross-sectional views of a damascene interconnect at different stages of integrated circuit fabrication.

DETAILED DESCRIPTION

FIG. 1 is a schematic representation of a wafer processing system 35 that can be used to perform integrated circuit metallization in accordance with the present invention. This apparatus typically comprises process chambers 36, 38, 40, 41, degas chambers 44, load-lock chambers 46, transfer chambers 48, 50, pass-through chambers 52, a microprocessor controller 54, along with other hardware components such as power supplies (not shown) and vacuum pumps (not shown). An example of such a wafer processing system 35 is an ENDURA® System commercially available from Applied Materials, Inc., Santa Clara, California.

Details of the wafer processing system 35 used in the present invention are described in commonly assigned U. S. Patent No. 5,186,718, entitled "Staged-Vacuum Substrate Processing System and Method", issued on February 16, 1993, and is hereby incorporated by reference. The salient features of this system 35 are briefly described below.

The wafer processing system 35 includes two transfer chambers 48, 50 each containing a transfer robot 49, 51. The transfer chambers 48, 50 are separated one from the other by pass through chambers 52.

Transfer chamber 48 is coupled to load-lock chambers 46, degas chambers 44, pre-clean chamber 42, and pass through chambers 52. Substrates (not shown) are loaded into the wafer processing system 35 through load-lock chambers 46. Thereafter, the substrates are sequentially degassed and cleaned in degas chambers 44 and the pre-clean chamber 42, respectively. The transfer robot 48 moves the substrates between the degas chambers 44 and the pre-clean chamber 42.

Transfer chamber 50 is coupled to a cluster of process chambers 36, 38, 40, 41. The cleaned substrates are moved from transfer chamber 48 into transfer chamber 50 via pass through chambers 52. Thereafter, transfer robot 51 moves the substrates between one or more of the process chambers 36, 38, 40, 41.

The process chambers 36, 38, 40, 41 are used to perform various integrated circuit fabrication sequences. For example, process chambers 36, 38, 40, 41 may include physical vapor deposition (PVD) chambers, ionized metal plasma physical vapor deposition (IMP PVD) chambers, chemical vapor deposition (CVD) chambers, and anti-reflective coating (ARC) chambers, among others.

FIG. 2 depicts a schematic cross-sectional view of a sputtering-type physical vapor deposition (PVD) process chamber 36 of wafer processing system 35. An example of such a PVD process chamber 36 is an IMP VECTRA™ chamber commercially available from Applied Materials, Inc., Santa Clara, California.

The PVD chamber 36 is coupled to a gas source 104, a pump system 106 and a target power source 108. The PVD chamber 36 encloses a target 110, a substrate 120 positioned on a vertically movable pedestal 112, and a shield 114 enclosing a reaction zone 118. A lift mechanism 116 is coupled to the pedestal 112 to position the pedestal 112 relative to the target 110.

The gas source 104 supplies a process gas into the PVD chamber 36. The process gas generally includes argon (Ar) or some other inert gas. The pump system 106 controls the pressure within the PVD chamber 36.

The target 110 is typically suspended from the top of the PVD chamber 36. The target 110 includes a material that is sputtered during operation of the wafer processing system 35. Although the target 110 may comprise, as a material to be deposited, an insulator or semiconductor, the target 110 generally comprises a metal. For example, the target 110 may be formed of aluminum (Al), copper (Cu), tantalum (Ta), niobium (Nb), vanadium (V) and combinations thereof as well as other materials known in the art.

The pedestal 112 supports the substrate 120 within the PVD chamber 36. The pedestal 112 is generally disposed at a fixed distance from the target 110 during processing. However, the distance between the target 110 and the substrate 120 may also be varied during processing. The pedestal 112 is supported by the lift mechanism 116, which moves the pedestal 112 along a range of vertical motion within the PVD chamber 36.

The PVD chamber 36 may comprise additional components for improving the deposition of sputtered particles onto the substrate 120. For example, the PVD chamber 36 may include an additional bias power source 124 for biasing the substrate 120. The bias power source 124 is coupled to the pedestal 112 for controlling the deposition of the film 122 onto the substrate 120. The power source 124 is typically an AC source having a frequency of, for example,
about 400 kHz.

The PVD chamber 36 may also comprise a magnet 126 or magnetic sub-assembly positioned behind the target 110 for creating a magnetic field proximate to the target 110. The PVD chamber 36 may also comprise a coil 130 proximately disposed within the shield 114, but between the target 110 and the substrate 112. The coil 130 may comprise either a single-turn coil or multi-turn coil that, when energized, ionizes the sputtered particles. The process is known as Ion Metal Plasma (IMP) deposition. The coil 130 is generally connected to an AC source 132 having a frequency of, for example, about 2 MHz.

The target power source 108 that is used to infuse the process gas with energy may comprise a DC source, a radio frequency (RF) source, or a DC-pulsed source. Applying

either DC or RF power in this manner creates an electric field in the reaction zone 118. The electric field ionizes the process gas in the reaction zone 118 to form a plasma comprising process gas ions, electrons and process gas atoms (neutrals). Additionally, the electric field accelerates the process gas ions toward the target 110 for sputtering target particles from the target 110. If electrons in the plasma collide into the sputtered target particles, these target particles become ionized.

This configuration enables deposition of sputtered and ionized target particles from the target 110 onto the substrate 120 to form a film 122 thereon. The shield 114 confines the sputtered particles and non-reactant gas in a reaction zone 118 within the PVD chamber 36. As such, the shield 114 prevents deposition of target particles in unwanted locations, for example, beneath the pedestal 112 or behind the target 110.

Once the bias power source 124 is applied, electrons in the plasma quickly accumulate to the substrate, creating a negative DC offset on the substrate 120 and the pedestal 112. The negative bias at the substrate 120 attracts sputtered target particles that become ionized. The target particles are generally attracted to the substrate 120 in a direction that is substantially orthogonal to the substrate 120. As such, the bias power source 124 enhances deposition of target particles over an unbiased substrate 120.

To improve the coverage and distribution of sputtered target material along the sidewalls within a substrate via or trench, the separation distance between the target 110 and substrate 120 is minimal, such as, for example, about 50 millimeters. The close proximity between the target 110 and the substrate 120 minimizes the possibility of these collisions within the reaction zone 118, while maximizing the collisions that occur within the trenches and vias on the substrate 120. The collisions of the sputtered target particles with the process gas atoms and ions within the vias or trenches redirects the target particles toward the sidewalls, thereby increasing the rate of deposition of the target material on the sidewalls.

FIG. 3 depicts a schematic cross-sectional view of a chemical vapor deposition (CVD) process chamber 38 of wafer processing system 35. Examples of such CVD process chambers 36 include TXZ™ chambers and WXZ™ chambers, commercially available from Applied Materials, Inc., Santa Clara, California.

The CVD process chamber 38 generally houses a wafer support pedestal 250, which is used to support a substrate 290. The wafer support pedestal 250 can typically be moved in a vertical direction inside the CVD process chamber 38 using a displacement mechanism (not shown). Depending on the specific CVD process, the substrate 290 can be heated to some desired temperature prior to or during deposition. For example, the wafer support pedestal 250 is heated by an embedded heater element 270. The pedestal may be resistively heated by applying an electric current from an AC power supply 206 to the heater element 270. The substrate 290 is, in turn, heated by the pedestal 250. A temperature sensor 272, such as a thermocouple, is also embedded in the wafer support pedestal 250 to monitor the temperature of the pedestal 250 in a conventional manner. The measured temperature is used in a feedback loop to control the AC power supply 206 for the heating element 270, such that the substrate temperature can be maintained or controlled at a desired temperature which is suitable for the particular process application. The pedestal 250 is optionally heated using a plasma or by radiant heat (not shown).

A vacuum pump 202, is used to evacuate the CVD process chamber 38 and to maintain the proper gas flows and pressures inside the chamber 38. A showerhead 220, through which process gases are introduced into the chamber 38, is located above the wafer support pedestal 250. The showerhead 220 is connected to a gas panel 230, which controls and supplies various gases provided to the chamber 38.

Proper control and regulation of the gas flows through the gas panel 230 is performed by mass flow controllers and a microprocessor controller 54. The showerhead 220 allows process gases from the gas panel 230 to be uniformly introduced and distributed in the CVD process chamber 38.

The showerhead 220 and wafer support pedestal 250 may also form a pair of spaced apart electrodes. When an electric field is generated between these electrodes, the process gases introduced into the chamber 38 are ignited into a plasma. Typically, the electric field is generated by connecting the wafer support pedestal 250 to a source of radio frequency (RF) power (not shown) through a matching network (not shown). Alternatively, the RF

power source and matching network may be coupled to the showerhead 220, or coupled to both the showerhead 220 and the wafer support pedestal 250.

Referring to FIG. 1, both the PVD process chamber 36 and the CVD process chamber 38 as described above are controlled by a microprocessor controller 54. The microprocessor controller 54 may be one of any form of general purpose computer processor that can be used in an industrial setting for controlling various chambers and sub-processors. The computer may use any suitable memory, such as random access memory, read only memory, floppy disk drive, hard disk, or any other form of digital storage, local or remote. Various support circuits may be coupled to the CPU for supporting the processor in a conventional manner. Software routines as required may be stored in the memory or executed by a second CPU that is remotely located.

The software routines are executed after the substrate is positioned on the pedestal. The software routine, when executed, transforms the general purpose computer into a specific process computer that controls the chamber operation so that the deposition process is performed. Alternatively, the process of the present invention may be performed in hardware, as an application specific integrated circuit or other type of hardware implementation, or a combination of software and hardware.

Barrier/Metal Layer Deposition

The present invention provides a method for metallizing integrated circuits. In one aspect, an integrated circuit is metallized by depositing liner material on a substrate followed by one or more metal layers. The liner material is selected from tantalum (Ta), tantalum nitride (TaN), niobium (Nb), niobium nitride (NbN), vanadium (V), vanadium nitride (VN), and combinations thereof. The liner material is preferably conformably deposited on the substrate using physical vapor deposition (PVD).

Nitrogen is provided to the PVD deposition chamber when nitride based liner material is to be formed. Also, an inert gas such as helium (He) or argon (Ar) may be provided to the PVD deposition chamber to maintain such chamber within the desired chamber pressure.

In general, the following deposition process parameters can be used to deposit the liner material. The process parameters range from a wafer temperature of about 20 °C to about 300 °C, a chamber pressure of about 0.5 millitorr to about 20 millitorr, and a DC power of between about 1 kilowatt to about 80 kilowatts.

After the liner material is deposited on the substrate, one or more layers of a metal are formed thereon. The one or more metal layers are conformably deposited on the liner material using chemical vapor deposition (CVD), physical vapor deposition (PVD), or a combination of both CVD and PVD. Typically, a CVD deposited metal layer (thickness in a range of about 200 Å to about 10,000 Å) is formed conformably on the barrier layer followed by a PVD deposited metal layer.

The one or more metal layers are preferably selected from copper, aluminum, tungsten, or other conductive material, as well as combinations thereof. For the PVD process, aluminum, tungsten or copper targets are used.

In general, the following process parameters can be used to form the PVD metal layer. The process parameters range from a wafer temperature of about 20 °C to about 700 °C, a chamber pressure of about 0.5 millitorr to about 20 millitorr, and a DC power of between about 1 kilowatt to about 80 kilowatts. Also, a gas such as hydrogen (H_2) or argon (Ar) may be provided to the PVD deposition chamber to maintain such chamber within the desired chamber pressure.

For the CVD process, an aluminum (Al) layer may be deposited from a reaction of a gas mixture containing dimethyl aluminum hydride (DMAH) and hydrogen (H_2) or argon (Ar) or other DMAH containing compounds. A CVD tungsten (W) layer may be deposited from a gas mixture containing tungsten hexafluoride (WF_6). A CVD copper (Cu) layer may be deposited from a gas mixture containing $Cu^{+2}(hfac)_2$ (copper hexafluoro acetylacetonate), $Cu^{+2}(fod)_2$ (copper heptafluoro dimethyl octanediene), Cu^{+1}hfac TMVS (copper hexafluoro acetylacetonate trimethylvinylsilane), or combinations thereof.

In general, the following process parameters can be used to form the CVD metal layer. The process parameters range from a wafer temperature of about 150 °C to about 350 °C, a chamber pressure of about 2 torr to about 30 torr, and a gas mixture flow rate of about 500 sccm to about

10,000 sccm.

The above process parameters are suitable for implementation on a 200 mm (millimeter) substrate in a deposition chamber available from Applied Materials, Inc. Other deposition chambers are within the scope of the invention, and the parameters listed above may vary according to the particular deposition chambers used to deposit the liner material as well as the one or more metal layers. For example, other deposition chambers may have a larger (e. g., configured to accommodate 300 mm substrates) or smaller volume, requiring gas flow rates, or powers that are larger or smaller than those recited for deposition chambers available from Applied Materials, Inc.

Liner materials selected from Ta, TaN, Nb, NbN, V, and VN generate overlying metal films of aluminum and copper with strong <111> grain orientation. Strong <111> grain orientation is characteristic of films with good electromigration reliability.

Integrated Circuit Fabrication

Damascene Interconnect

FIGS. 4a-4d illustrate schematic cross-sectional views of a substrate 300 at different stages of a damascene interconnect fabrication sequence. Depending on the specific stage of processing, substrate 300 may correspond to a silicon substrate, or other material layer that has been formed on the substrate 300. FIG. 4a, for example, illustrates a cross-sectional view of a substrate 300 having a dielectric layer 302 thereon. The dielectric layer 302 may be an oxide (e. g., silicon dioxide, fluorosilicate glass). In general, the substrate 300 may include a layer of silicon, silicides, metals, or other materials.

FIG. 4a illustrates one embodiment in which the substrate 300 is silicon having a fluorosilicate glass layer formed thereon. The dielectric layer has a thickness of about 10,000 Å to about 20,000 Å, depending on the size of the structure to be fabricated.

The dielectric layer 302 has apertures 306 therethrough. The apertures 306 have dimensions less than about 0.5 μm (micrometer), providing aspect ratio structures in the range of about 3:1 to about 4:1.

Referring to FIG. 4b, liner material 304 is conformably deposited on the dielectric layer 302. The liner material 304 is conformably deposited on the dielectric layer according to the process parameters described above. The liner material is selected from Ta, TaN, Nb, NbN, V, VN, or combinations thereof.

The thickness of the liner material 304 is variable depending on the specific stage of processing. Typically, the liner material 304 has a thickness of about 200 Å to about 600 Å.

After the liner material 304 is deposited conformably on the dielectric layer 302, a CVD metal layer 308 is formed thereon, as depicted in FIG. 4c. The CVD metal layer 308 is selected from Al, Cu, or combinations thereof. The CVD metal layer 308 has a thickness of about 200 Å to about 10,000 Å.

Referring to FIG. 4d, the damascene interconnect is completed with the filling of the apertures with a PVD metal layer 310. The PVD metal layer 310 is selected from Al, Cu, or combinations thereof. The PVD metal layer 310 has a thickness of about 2000 Å to about 10,000 Å.

Although several preferred embodiments, which incorporate the teachings of the present invention, have been shown and described in detail, those skilled in the art can readily devise many other varied embodiments that still incorporate these teachings.

What is claimed is:

1. A device, comprising:

a substrate;

liner material conformably deposited on the substrate, wherein the liner material is selected from tantalum (Ta), tantalum nitride (TaN), niobium (Nb), niobium nitride (NbN), vanadium (V), vanadium nitride (VN), and combinations thereof; and

one or more metal layers conformably deposited over the liner material.

2. The device of claim 1 wherein the substrate has one or more material layers formed thereon.

3. The device of claim 2 wherein the one or more material layers are selected from fluorinated silicate glass (FSG), oxynitride, silicon oxide and combinations thereof.

4. The method of claim 2 wherein the one or more material layers have apertures formed therein.

5. The device of claim 4 wherein the apertures are formed through the one or more material layers to the substrate surface.

6. The device of claim 4 wherein the apertures each have dimensions less than about 1 μm (micrometer).

7. The device of claim 1 wherein the liner material has a thickness in a range of about 50 Å to about 1000 Å.

8. The device of claim 1 wherein the one or more metal layers are selected from aluminum (Al), copper (Cu), tungsten (W), and combinations thereof.

9. A damascene interconnect, comprising:

a substrate;

one or more dielectric layers formed on the substrate, wherein the one or more dielectric layers have apertures therein;

liner material conformably deposited on the surfaces of the apertures, wherein the liner material is selected from tantalum (Ta), tantalum nitride (TaN), niobium (Nb), niobium nitride (NbN), vanadium (V), vanadium nitride (VN), and combinations thereof; and

one or more metal layers conformably deposited on the liner.

10. The damascene interconnect of claim 9 wherein the substrate has one or more layers formed thereon.

11. The damascene interconnect of claim 9 wherein the one or more dielectric layers are selected from the group of fluorinated silicate glass (FSG), oxynitride, silicon nitride and combinations thereof.

12. The damascene interconnect of claim 9 wherein the apertures are formed through the one or more dielectric layers to the substrate surface.

13. The damascene interconnect of claim 9 wherein the apertures each have dimensions less than about 1 μm (micrometer).

14. The damascene interconnect of claim 9 wherein the liner material has a thickness in a range of about 50 Å to about 1000 Å.

15. The damascene interconnect of claim 9 wherein the one or more metal layers are selected from aluminum (Al), copper (Cu), and combinations thereof.

16. A method of fabricating a device, comprising:

depositing liner material conformably on a substrate, wherein the liner material is selected from tantalum (Ta), tantalum nitride (TaN), niobium (Nb), niobium nitride (NbN), vanadium (V), vanadium nitride (VN) and combinations thereof; and

depositing one or more metal layers conformably on the liner material.

17. The method of claim 16 wherein the substrate has one or more material layers thereon.

18. The method of claim 17 wherein the one or more material layers are selected from the group of fluorinated silicate glass (FSG), oxynitride, silicon oxide and combinations thereof.

19. The method of claim 17 wherein the one or more material layers have apertures therein.

20. The method of claim 19 wherein the apertures are formed through the one or more material layers to the substrate surface.

21. The method of claim 19 wherein the apertures each have dimensions less than about 1 μm (micrometer).

22. The method of claim 16 wherein the liner material has a thickness in a range of about 50 Å to about 1000 Å.

23. The method of claim 16 wherein the one or more metal layers are selected from aluminum (Al), copper (Cu), tungsten (W), and combinations thereof.

24. The method of claim 16 wherein the liner material is deposited on the substrate by

positioning the substrate in a deposition chamber enclosing a target, wherein the target comprises liner material; and

generating a plasma in the deposition chamber, wherein the plasma comprises ionized particles that sputter liner material from the target onto the substrate to deposit the liner material thereon.

25. The method of claim 24 wherein the deposition chamber is maintained at a pressure between about 0.5 millitorr to about 20 millitorr.

26. The method of claim 24 wherein the deposition chamber is maintained at a temperature between about 20 °C to about 300 °C.

27. The method of claim 24 wherein the plasma is generated by applying a DC power and a magnetic field to the target.

28. The method of claim 27 wherein the DC power is in a range of about 1 kilowatt to about 80 killowatts.

29. The method of claim 16 wherein the one or more metal layers are formed on the liner material by

positioning the substrate in a deposition chamber;

providing a gas mixture to the deposition chamber; and

thermally decomposing the gas mixture provided to the deposition chamber to form the one or more metal layers on the liner material.

30. The method of claim 29 wherein the gas mixture comprises dimethyl aluminum hydride (DMAH), DMAH containing compounds, tungsten hexafluoride (WF_6), hydrogen (H_2), $Cu^{+2}(hfac)_2$ (copper hexafluoro acetylacetonate), $Cu^{+2}(fod)_2$ (copper heptafluoro dimethyl octanediene), Cu^{+1}hfac TMVS (copper hexafluoro acetylacetonate trimethylvinylsilane), or combinations thereof.

31. The method of claim 29 wherein the deposition chamber is maintained at a pressure between about 2 torr to about 30 torr.

32. The method of claim 29 wherein the deposition chamber is maintained at a temperature between about 150 °C to about 350 °C.

33. The method of claim 16 wherein at least one of the one or more metal layers are formed on the liner material by

positioning the substrate in a deposition chamber enclosing a target, wherein the target comprises a metal; and

generating a plasma in the deposition chamber wherein, the plasma comprises ionized particles that sputter metal from the target onto the substrate to form the metal layer thereon.

34. The method of claim 33 wherein the plasma is generated by applying a DC power and a magnetic field to the target.

35. The method of claim 34 wherein the DC power is in a range of about 1 kilowatt to about 80 kilowatts.

36. A method of fabricating a damascene interconnect, comprising:

providing a substrate with one or more dielectric layers thereon, wherein the one or more dielectric layers have apertures therein;

depositing liner material conformably on the surfaces of the apertures, wherein the liner material is selected from tantalum (Ta), tantalum nitride (TaN), niobium (Nb), niobium nitride (NbN), vanadium (V), vanadium nitride (VN), and combinations thereof; and

depositing one or more metal layers conformably on the liner.

37. The method of claim 36 wherein the substrate has one or more material layers formed thereon.

38. The method of claim 36 wherein the one or more dielectric layers are selected from the group of fluorinated silicate glass (FSG), oxynitride, silicon oxide and combinations thereof.

39. The method of claim 36 wherein the apertures are formed through the one or more dielectric layers to the substrate surface.

40. The method of claim 36 wherein the apertures each have dimensions less than about 1 μm (micrometer).

41. The method of claim 36 wherein the liner material has a thickness in a range of about 50 Å to about 1000 Å.

42. The method of claim 36 wherein the one or more metal layers are selected from aluminum (Al), copper (Cu), and combinations thereof.

43. The method of claim 36 wherein the liner material is deposited on the surfaces of the one or more dielectric layers by

positioning the substrate in a deposition chamber enclosing a target, wherein the target comprises liner material; and

generating a plasma in the deposition chamber, wherein the plasma comprises ionized particles that sputter liner material from the target on the substrate to deposit the liner material thereon.

44. The method of claim 43 wherein the deposition chamber is maintained at a pressure between about 0.5 millitorr to about 20 millitorr.

45. The method of claim 43 wherein the deposition chamber is maintained at a temperature between about 20 °C to about 300 °C.

46. The method of claim 43 wherein the plasma is generated by applying a DC power and a magnetic field to the target.

47. The method of claim 46 wherein the DC power is in a range of about 1 kilowatt to about 80 kilowatts.

48. The method of claim 36 wherein the one or more metal layers are formed on the liner material by

positioning the substrate in a deposition chamber;

providing a gas mixture to the deposition chamber; and

thermally decomposing the gas mixture provided to the deposition chamber to form the one or more metal layers on the liner material.

49. The method of claim 48 wherein the gas mixture comprises dimethyl aluminum hydride (DMAH), DMAH containing compounds, hydrogen (H_2), $Cu^{+2}(hfac)_2$ (copper hexafluoro acetylacetonate), $Cu^{+2}(fod)_2$ (copper heptafluoro dimethyl octanediene), Cu^{+1}hfac TMVS (copper hexafluoro acetylacetonate trimethylvinylsilane), or combinations thereof.

50. The method of claim 48 wherein the deposition chamber is maintained at a pressure between about 2 torr to about 30 torr.

51. The method of claim 48 wherein the deposition chamber is maintained at a temperature between about 150 °C to about 350 °C.

52. The method of claim 36 wherein at least one metal layer of the one or more metal layers is deposited on the liner material by

positioning the substrate in a deposition chamber enclosing a target, wherein the target comprises a metal; and

generating a plasma in the deposition chamber, wherein the plasma comprises ionized particles that sputter metal from the target on the substrate to deposit the a metal layer thereon.

53. The method of claim 52 wherein the plasma is generated by applying a DC power and a magnetic field to the target.

54. The method of claim 53 wherein the DC power is in a range of about 1 kilowatt to about 80 kilowatts.

55. A computer storage medium containing a software routine that, when executed, causes a general purpose computer to control a deposition chamber using a method of thin film deposition comprising:

depositing liner material conformably on a substrate, wherein the liner material is selected from tantalum (Ta), tantalum nitride (TaN), niobium (Nb), niobium nitride (NbN), vanadium (V), vanadium nitride (VN) and combinations thereof; and

depositing one or more metal layers conformably on the liner material.

56. The computer storage medium of claim 55 wherein the liner material is deposited on the substrate by

positioning the substrate in a deposition chamber enclosing a target, wherein the target comprises liner material; and

generating a plasma in the deposition chamber, wherein the plasma comprises ionized particles that sputter liner material from the target onto the substrate to deposit the liner material thereon.

57. The computer storage medium of claim 56 wherein the deposition chamber is maintained at a pressure between about 0.5 millitorr to about 20 millitorr.

58. The computer storage medium of claim 56 wherein the deposition chamber is maintained at a temperature between about 20 °C to about 300 °C.

59. The computer storage medium of claim 56 wherein the plasma is generated by applying a DC power and a magnetic field to the target.

60. The computer storage medium of claim 59 wherein the DC power is in a range of about 1 kilowatt to about
80 kilowatts.

61. The computer storage medium of claim 55 wherein the one or more metal layers are formed on the liner material by

positioning the substrate in a deposition chamber;

providing a gas mixture to the deposition chamber; and

thermally decomposing the gas mixture provided to the deposition chamber to form the one or more metal layers on the liner material.

62. The computer storage medium of claim 61 wherein the deposition chamber is maintained at a pressure between about 2 torr to about 30 torr.

63. The computer storage medium of claim 61 wherein the deposition chamber is maintained at a temperature between about 150 °C to about 350 °C.

64. The computer storage medium of claim 55 wherein at least one of the one or more metal layers are formed on the liner material by

positioning the substrate in a deposition chamber enclosing a target, wherein the target comprises a metal; and

generating a plasma in the deposition chamber wherein the plasma comprises ionized particles that sputter metal from the target onto the substrate to form the metal layer thereon.

65. The computer storage medium of claim 64 wherein the plasma is generated by applying a DC power and a magnetic field to the target.

66. The computer storage medium of claim 65 wherein the DC power is in a range of about 1 kilowatt to about 80 kilowatts.

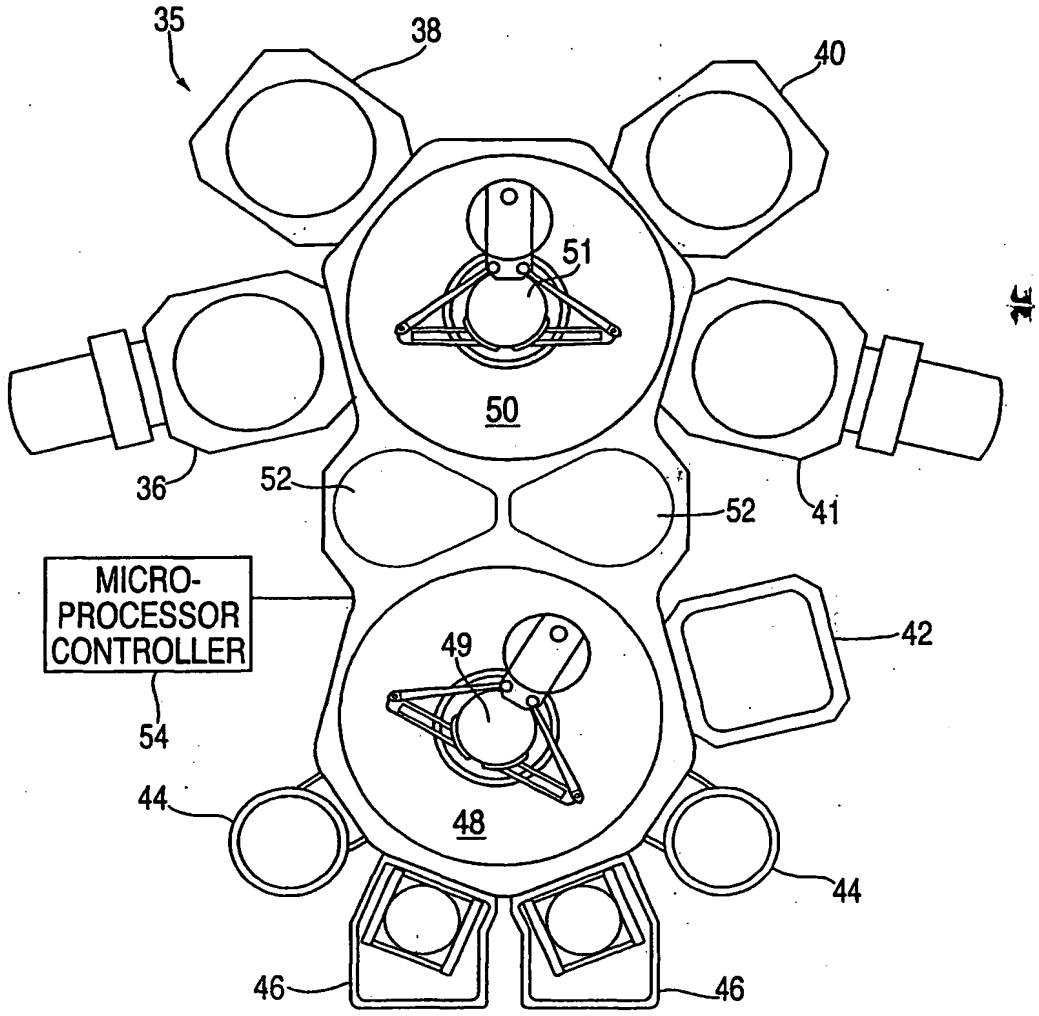
35
38
40
51
50
36
52
52
41
MICRO-
PROCESSOR
CONTROLLER
49
42
54
44
48
44
46
46

FIG. 1

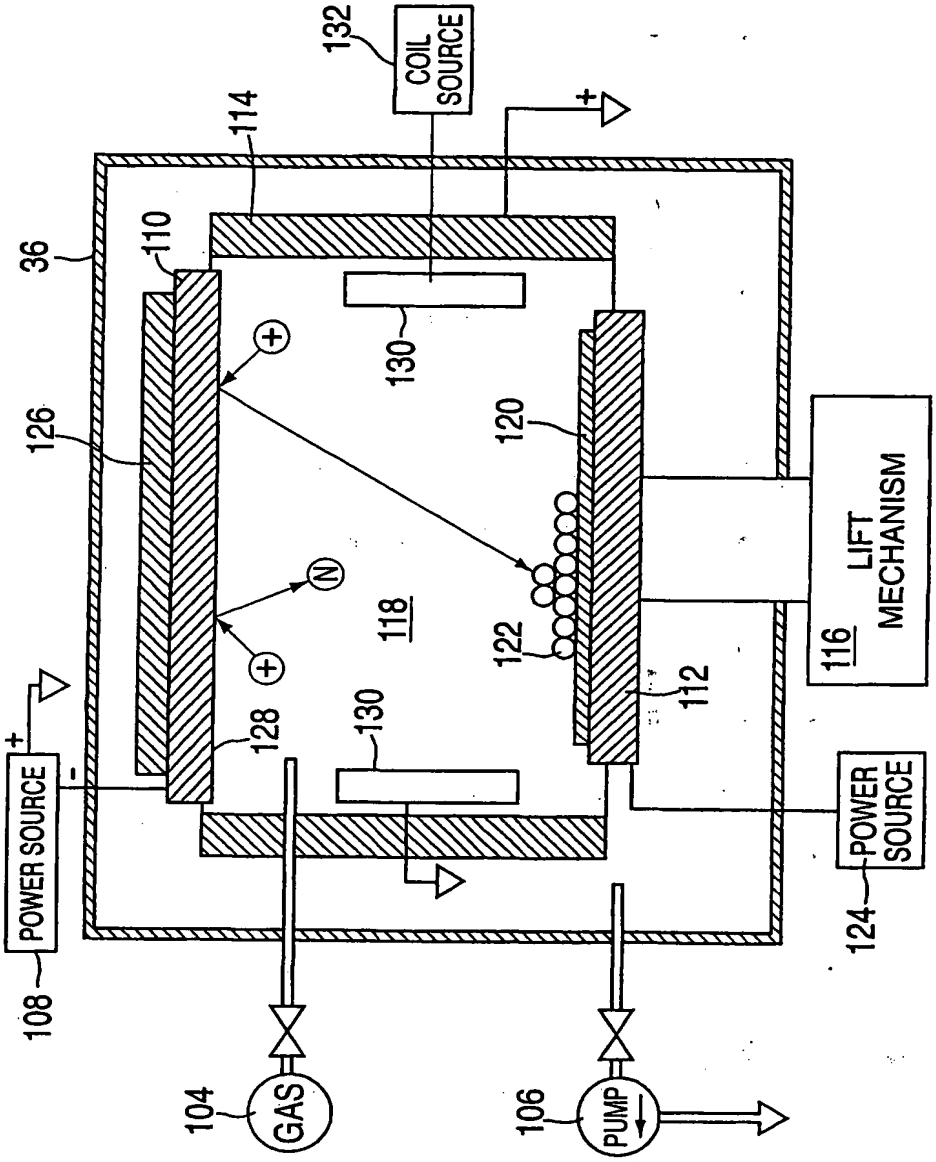
132
COIL SOURCE
114
36
110
130
126
120
LIFT MECHANISM
116
118
122
112
128
130
POWER SOURCE
POWER SOURCE
108
124
104
GAS
106
PUMP

FIG. 2

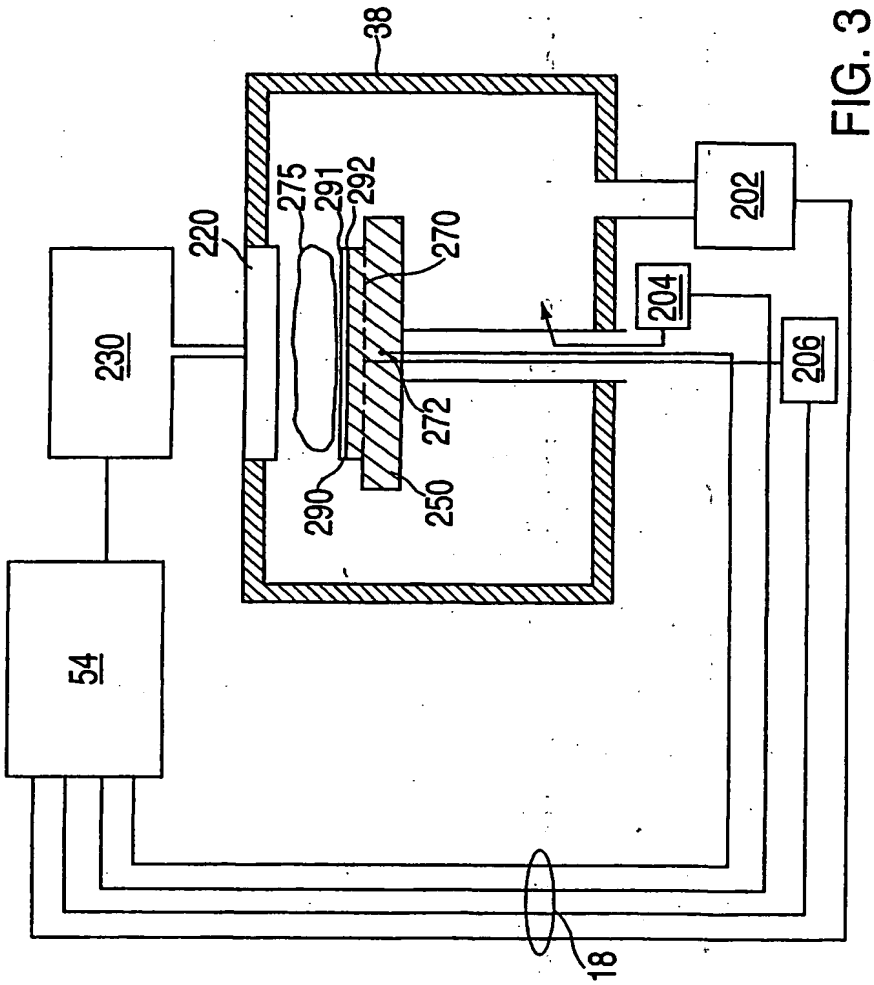

FIG. 3

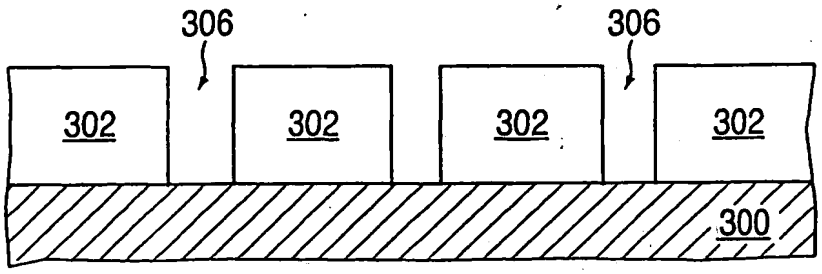

FIG. 4a

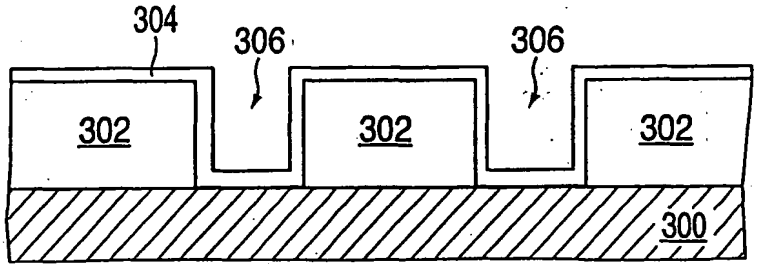

FIG. 4b

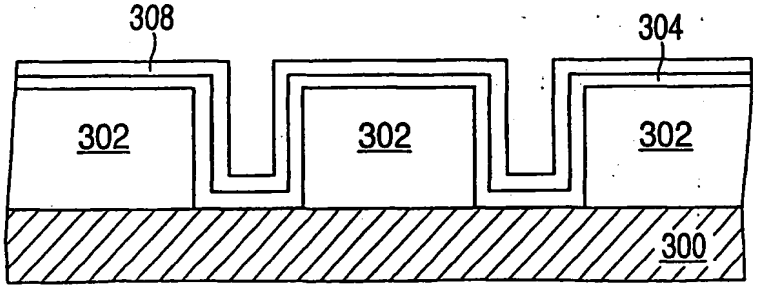

FIG. 4c

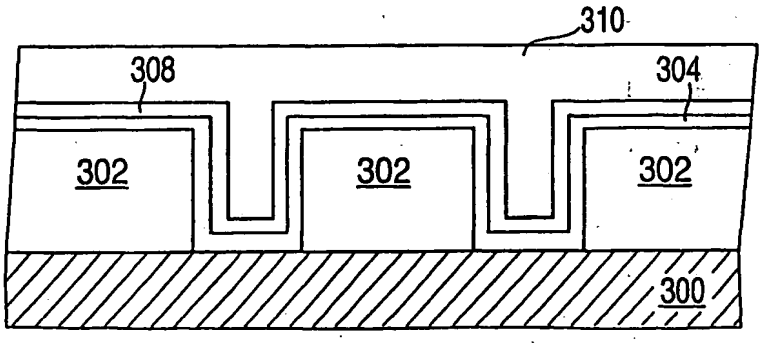

FIG. 4d